

Features

2 Meg x 8 bit CMOS Static

Random Access Memory

- Access Times 70 thru 100ns
- Data Retention Function (EDI8F82048LP)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

High Density Packaging

- 36 Pin SIP, No. 136
- 36 Pin Flat SIP, No. 335

Single +5V (±10%) Supply Operation

**2 Megabits x 8
Static RAM CMOS, Module**

The EDI8F82048C is a 16 megabit CMOS Static RAM based on sixteen 128Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

A low power version with data retention (EDI8F82048LP) is also available.

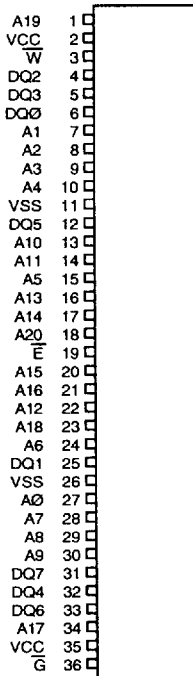
The EDI8F82048C is offered in a double sided, 36 pin single-in-line package (SIP), which provides a cost effective solution to very high packing density.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Fully asynchronous, the EDI8F82048C requires no clocks or refreshing for operation.

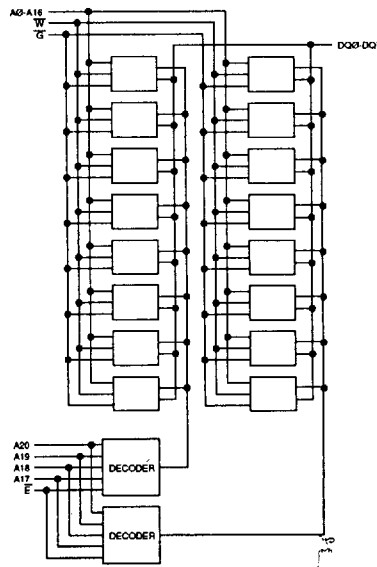
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Pin Configurations and Block Diagram



Pin Names

A0-A20	Address Inputs
\bar{E}	Chip Enable
\bar{W}	Write Enable
\bar{G}	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	TTL, CL = 100pF

(note: For TEHQZ, TGHQZ and TWLOZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power	ICC1	$\bar{W}, \bar{E} = VIL, I/O = 0mA,$	--		210	mA
Supply Current		Min Cycle				
Standby (TTL) Power	ICC2	$\bar{E} \geq VIH, VIN \leq VIL$	--		135	mA
Supply Current		$VIN \geq VIH$				
Full Standby Power	ICC3	$\bar{E} \geq VCC-0.2V$			20	mA
Supply Current (CMOS)		$VIN \geq VCC-0.2V$ or $VIN \leq 0.2V$			500	μA
			C			
			LP			
Input Leakage Current	ILI	$VIN = 0V$ to VCC	--	--	± 20	μA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC	--	--	± 20	μA
Output High Voltage	VOH	$I/OH = -1.0mA$	2.4	--	--	V
Output Low Voltage	VOL	$I/O L = 2.1mA$	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\bar{G}	\bar{E}	\bar{W}	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f = 1.0MHz, VIN = VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	110	pF
Data Lines	CD/Q	130	pF
Chip Enable and A17-A20 Lines	CC	20	pF

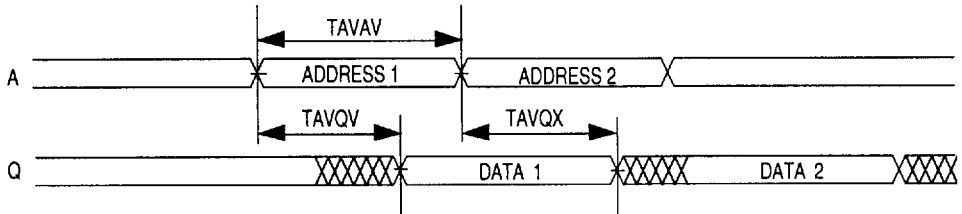
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

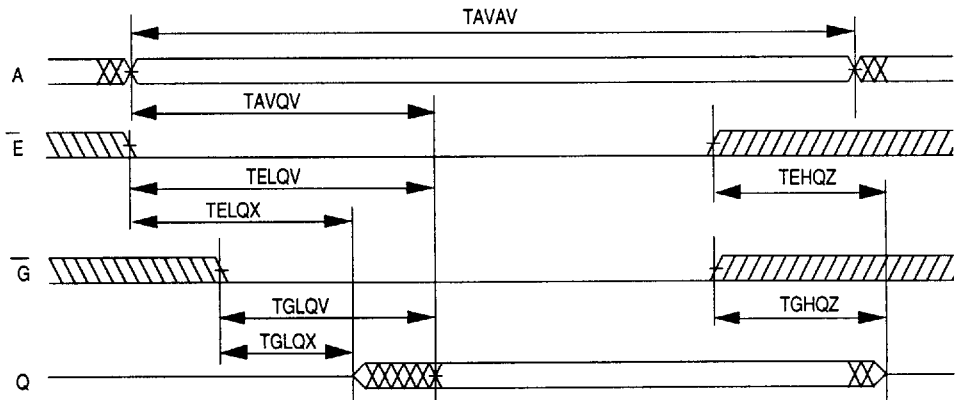
Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W High, \bar{G} , \bar{E} Low



Read Cycle 2 - W High



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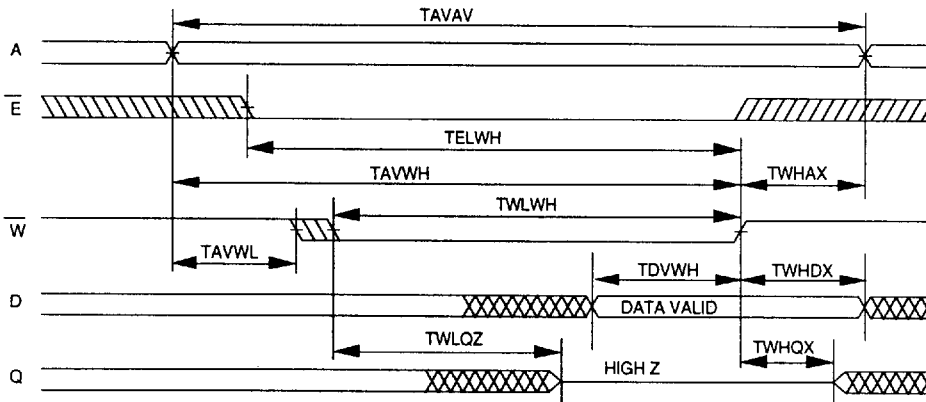


AC Characteristics Write Cycle

Write Cycle Parameter	Symbol	JEDEC AL	70ns		85ns		100ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	65		70		80		ns
	TELEH	TCW	65		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	65		70		80		ns
	TAVEH	TAW	65		70		80		ns
Write Pulse Width	TWLWH	TWP	65		70		80		ns
	TWLEH	TWP	65		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW	30		35		40		ns
	TDVEH	TDW	30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

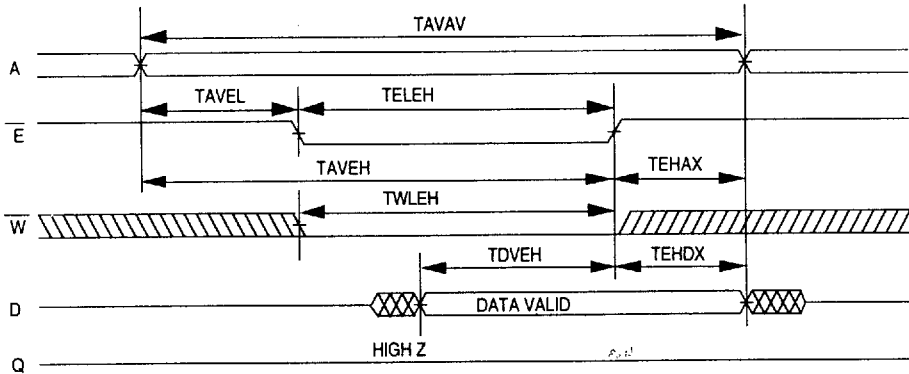
Write Cycle 1 - W Controlled



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ED18F82048C
2Megx8 SRAM Module

Write Cycle 2 - \bar{E} Controlled



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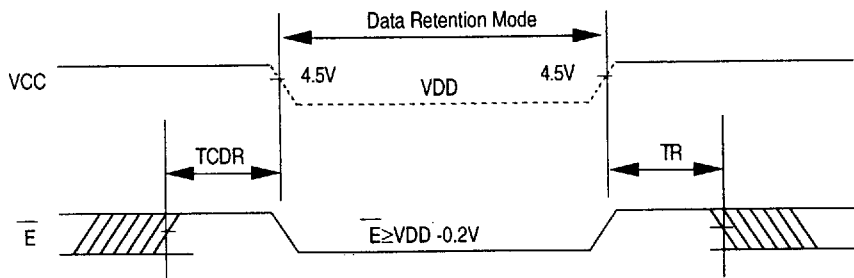
Data Retention Characteristics

LP Version Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	VDD	$\bar{E} \geq VDD - 0.2V$ $VIN \geq VDD - 0.2V$ or $VIN \leq 0.2V$		2	--	--	--	V
Data Retention Quiescent Current	ICCDR		2V	--		300	450	μA
			3V			400	550	μA
Chip Disable to Data Retention Time(1)	TCDR			0	--	--	--	ns
Operation Recovery Time (1)	TR		TAVAV*	--	--	--	ns	

Note 1: Parameter guaranteed, but not tested.
* Read Cycle Time

Data Retention - \bar{E} Controlled



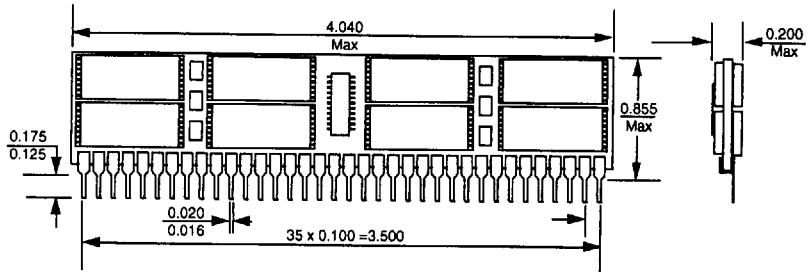
Ordering Information

Standard Power	Low Power with Data Retention	Speed (ns)	Package No.
EDI8F82048C70BSC	EDI8F82048LP70BSC	70	136
EDI8F82048C85BSC	EDI8F82048LP85BSC	85	136
EDI8F82048C100BSC	EDI8F82048LP100BSC	100	136
EDI8F82048C70BFC	EDI8F82048LP70BFC	70	335
EDI8F82048C85BFC	EDI8F82048LP85BFC	85	335
EDI8F82048C100BFC	EDI8F82048LP100BFC	100	335

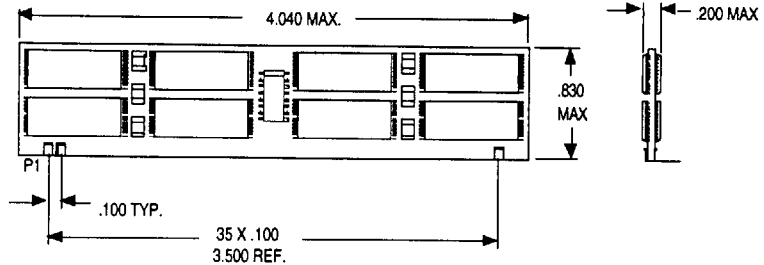
Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI8F82048C70BSC becomes EDI8F82048C70BSI.

Package Description

Package No. 136 36 Pin Single-in-line Package



Package No. 335 36 Pin Flat SIP



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